voltage, comprising:

a first insulated gate transistor receiving the first voltage at a gate thereof and having a first conduction node, and a second conduction node for outputting a difference signal;

a second insulated gate transistor receiving the second voltage at a gate thereof and having a first conduction node connected to said first conduction node of said first insulated gate transistor, said second insulated gate transistor having a current supply ability different from a current supply ability of said first insulated gate transistor under a condition of the same gate voltage, and said difference signal corresponding to a difference between the first and second voltages; and

a current mirror coupled to the first and second insulated gate transistors for supplying current to the first and second insulated gate transistors.

20. The level detection circuitry according to claim 19, wherein said first insulated gate transistor is smaller in channel width than said second insulated gate transistor.

21. The level detection circuitry according to claim 19, further comprising a buffer circuit for buffering said difference signal for generating a level detection signal indicating whether said first voltage is higher than said second voltage.

22. The level detection circuitry according to claim 19, wherein said first voltage is a power supply voltage, and said second voltage is a reference voltage for determining a voltage level of an internal voltage generated from said power supply voltage.--

REMARKS

The above amendments have been made in order to include the prior applications to the specification and to add new claims 19-22.

Entry of this Preliminary Amendment is respectfully requested.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Stephen A. Becker

Registration No. 26,527

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 SAB:blp
Date: November 15, 2001
Facsimile: (202) 756-8087